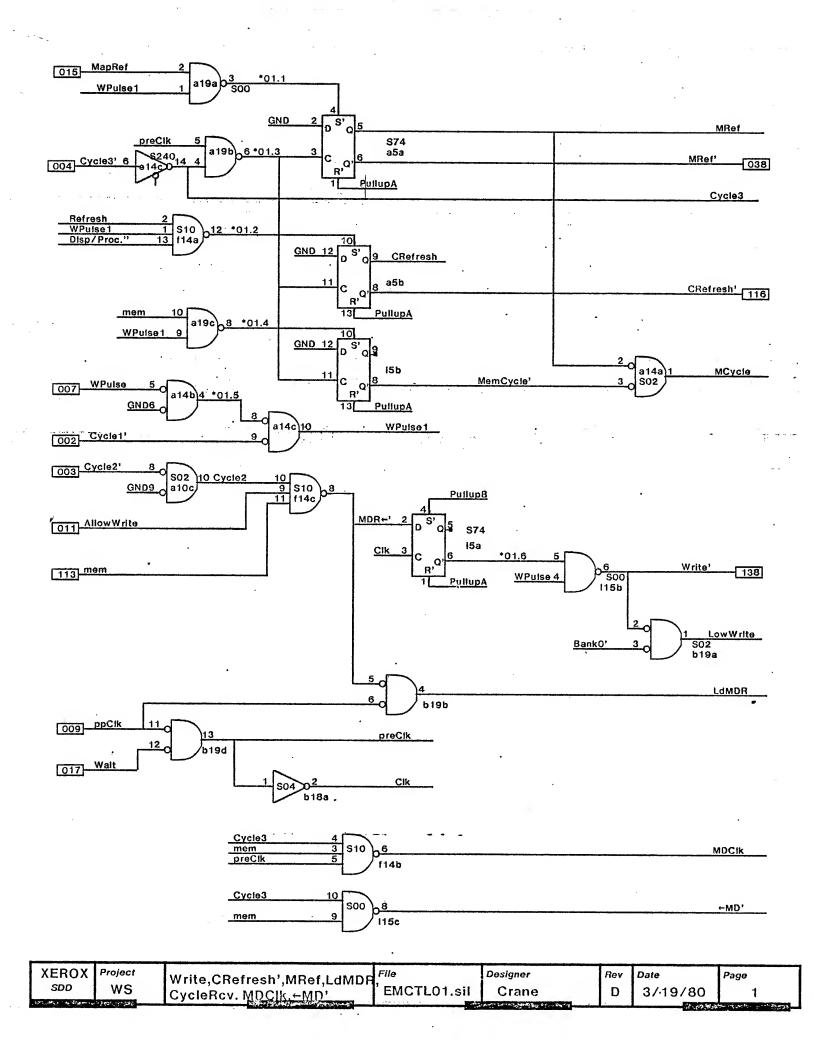
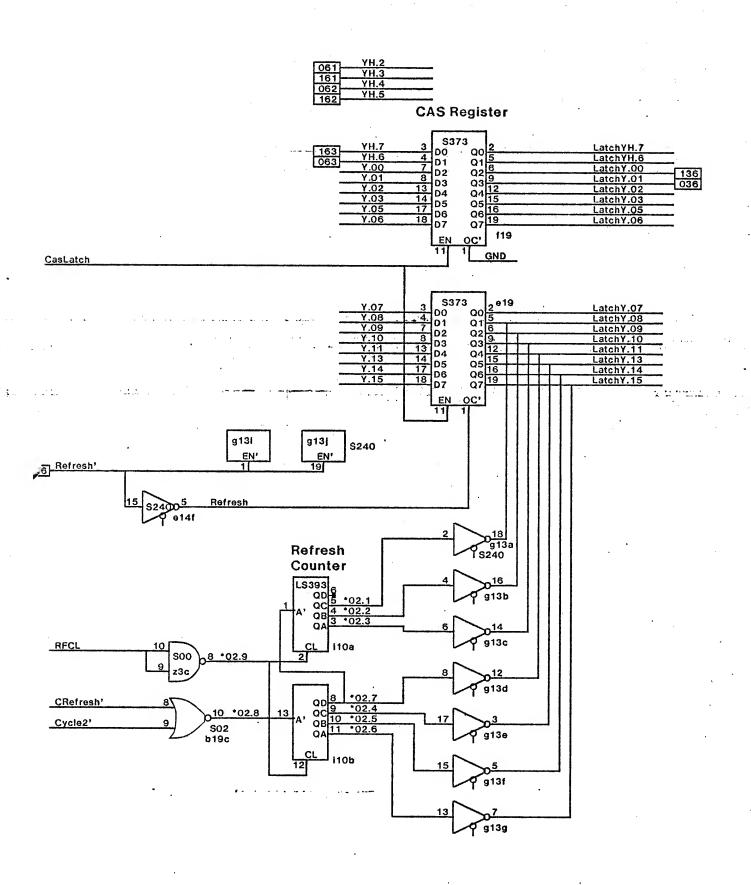
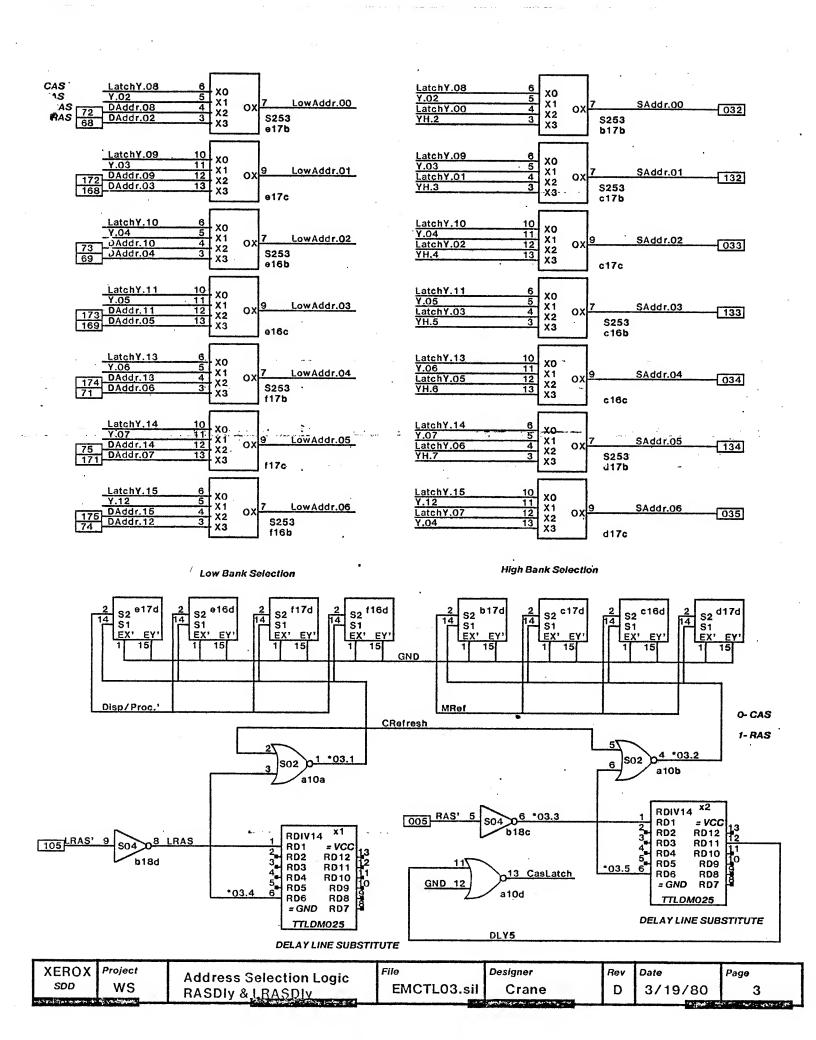
Memory Control Card,

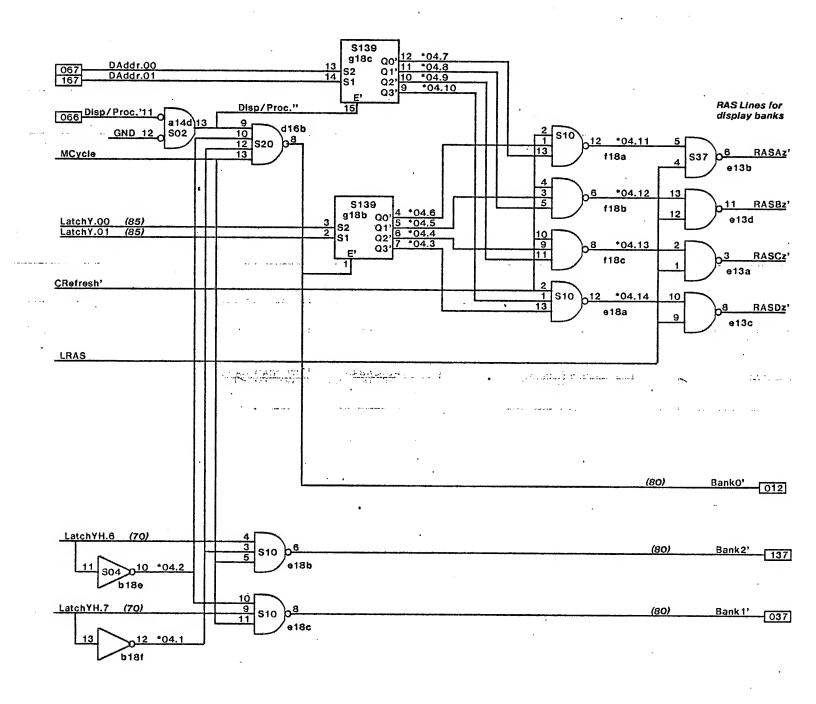
- 1. Write, CRefresh', MRef, LdMDR, Cycle Rcv., MDClk, ←MD'
- 2. Refresh Counter & Cas Registers
- 3. Address Selection Logic, RASDly, & LRASDly
- 4. Memory Bank Selection
- 5. Drivers for Address, CAS', & Write'
- 6. Low Bank A
- 7. Low Bank B
- 8. Low Bank C
- 9. Low Bank D
- 10. Mem. Data Register, Mem. Control Reg., Check bit Gen.
- 11. Memory Chip data paths
- 12. Memory Data Buffers
- 13. Syndrome Generator
- 14. Error Correction Data paths
- 15. Error Log Register
- 16. Resistors and R-Dips
- 17. Caps Diodes and Fuses
- 18. Test Points
- 19. Material List
- 20. Board Layout



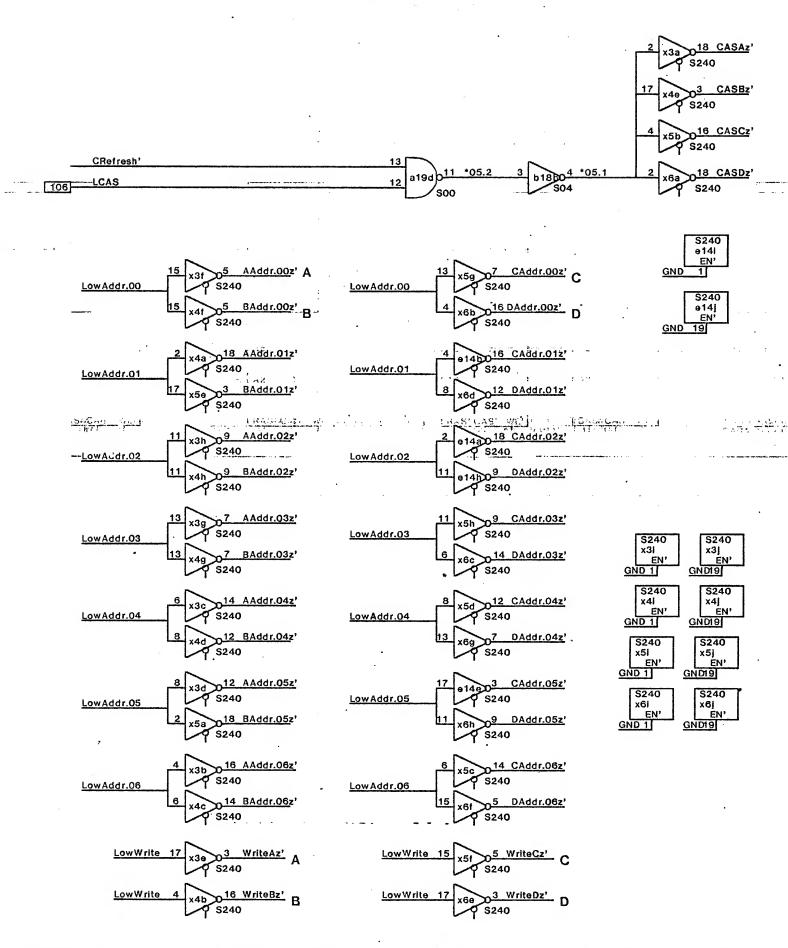


1	XEROX	Project	Refresh Counter &	File	Designer	Rev	Date	Page
	SDD	ws	CAS Registers	EMCTL02.sil	Crane	D	2/14/80	2
	tapping the law with	The state of the s	をおける 1 mm 1		the same of the same of the same of the same of		100	Fr State State Systems

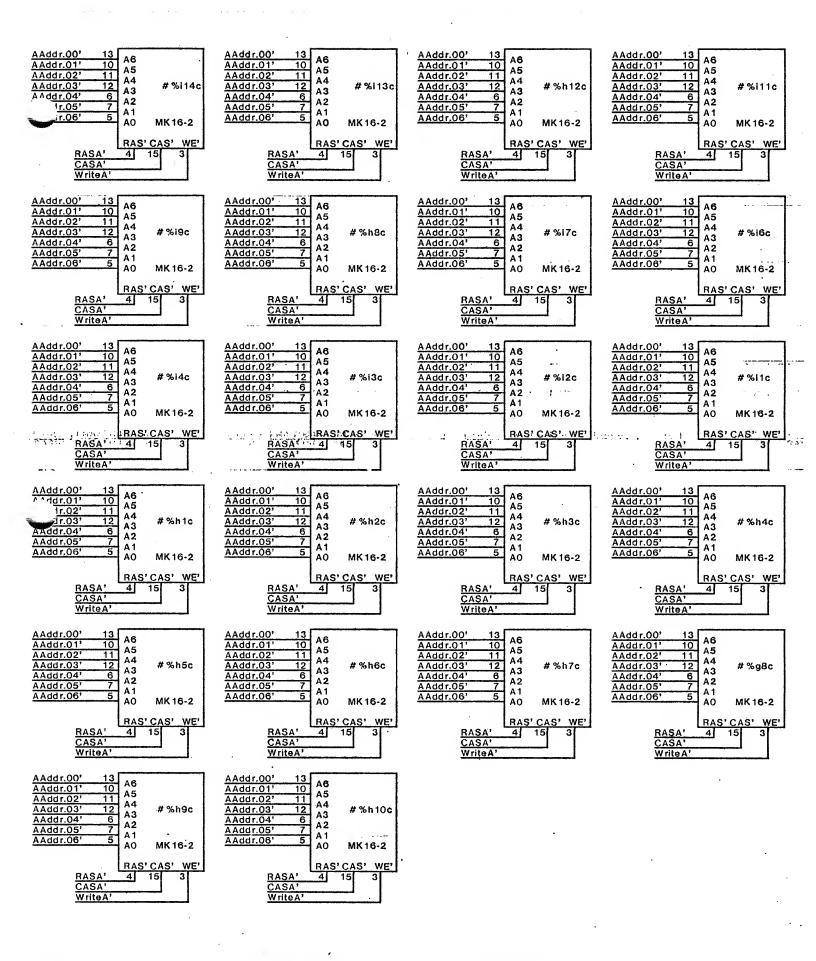




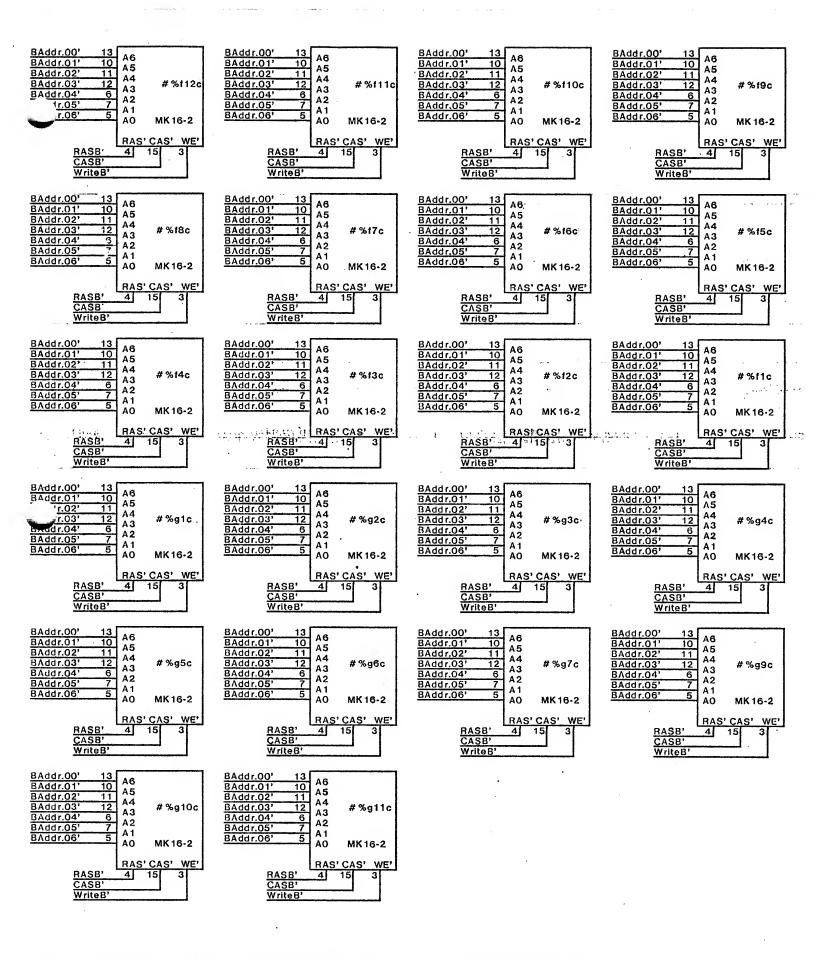
XEROX	Project		File	Designer	Rev	Date	Page
SDD	ws	Memory Bank Selection	EMCTL04.sil	Crane	D	3/19/80	4
and the broken to the second	A series and the seri	The Secreta Martin Comment		-			



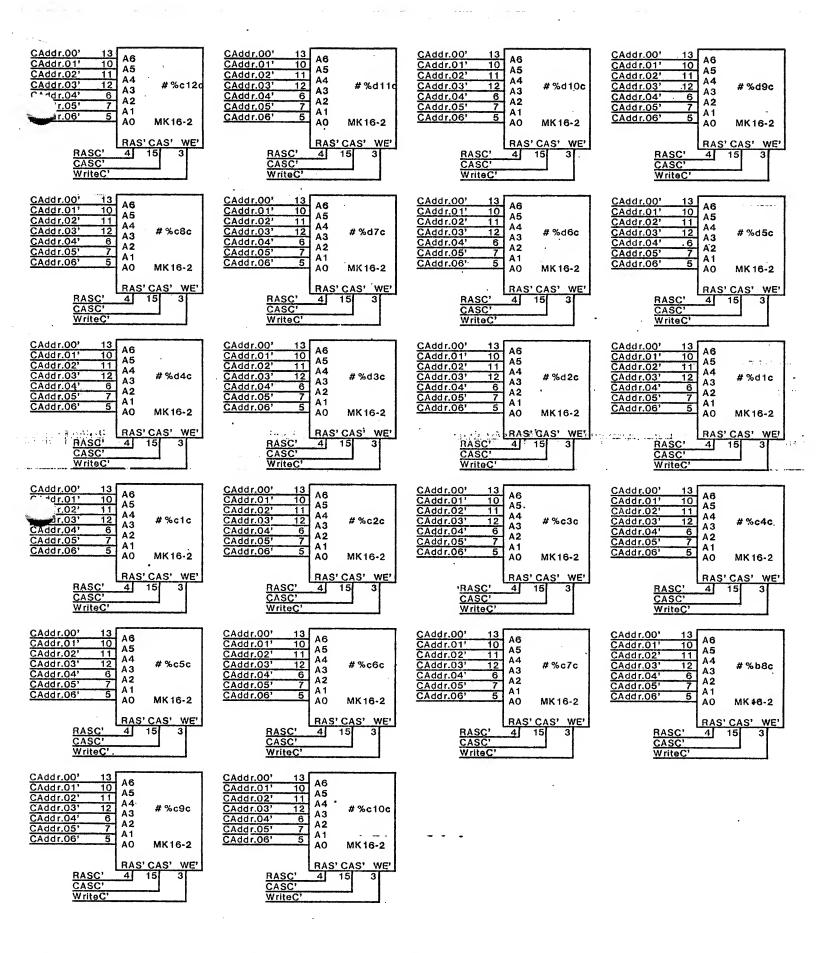
		man and the second					
XEROX	Project	Low 64K Bank Drivers	File	Designer	Rev	Date	Page
SDD	ws	for Address, CAS', & Write'	EMCTL05.sil	Crane/Cucinitti	ם	3/19/80	5
"Janate Malander, 1970)	U. Carrier	and the state of t	EXT	Marin Strange and Strange and St.		I the specification	to modify to



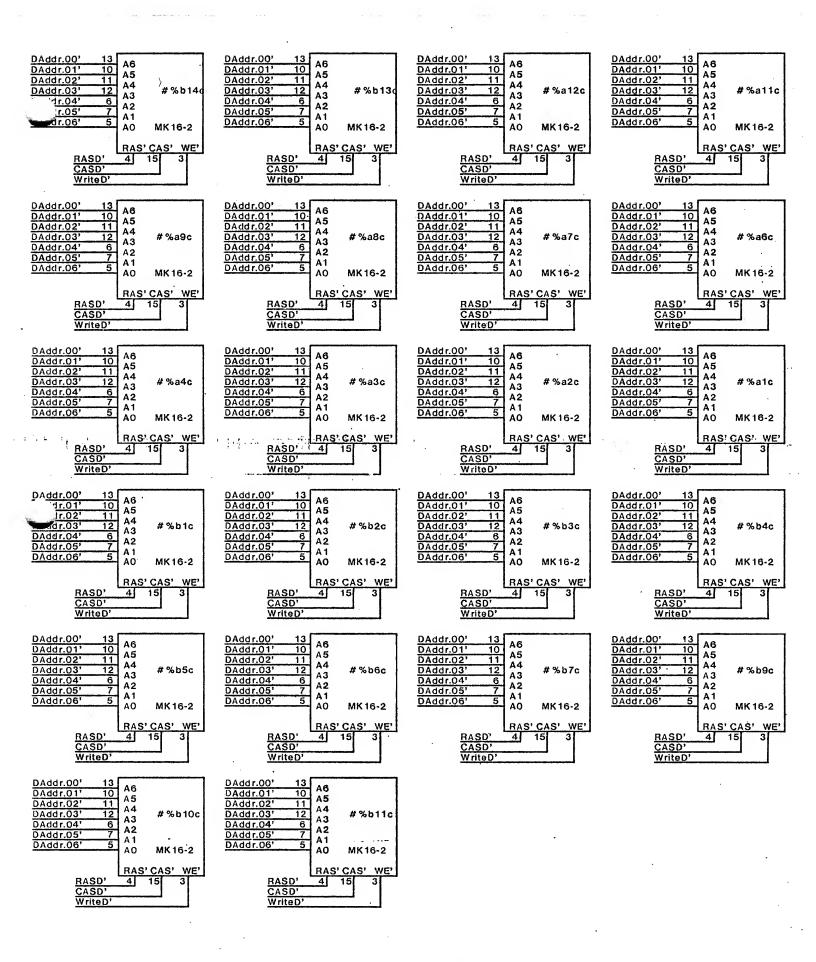
-	XEROX	Project		File	Designer	Rev	Date	Page
	SDD	WS	Mem. Control/ Low Bank A	EMCTL06.sil	JR Cucinitti	ם	2/14/80	6
1	Ten to age or the THINK TO	The second secon	the fact details for the fact of the fact	BN931	THE PERSON NAMED IN COLUMN TWO IS NOT THE OWNER.		70777	or a colorest condition of the



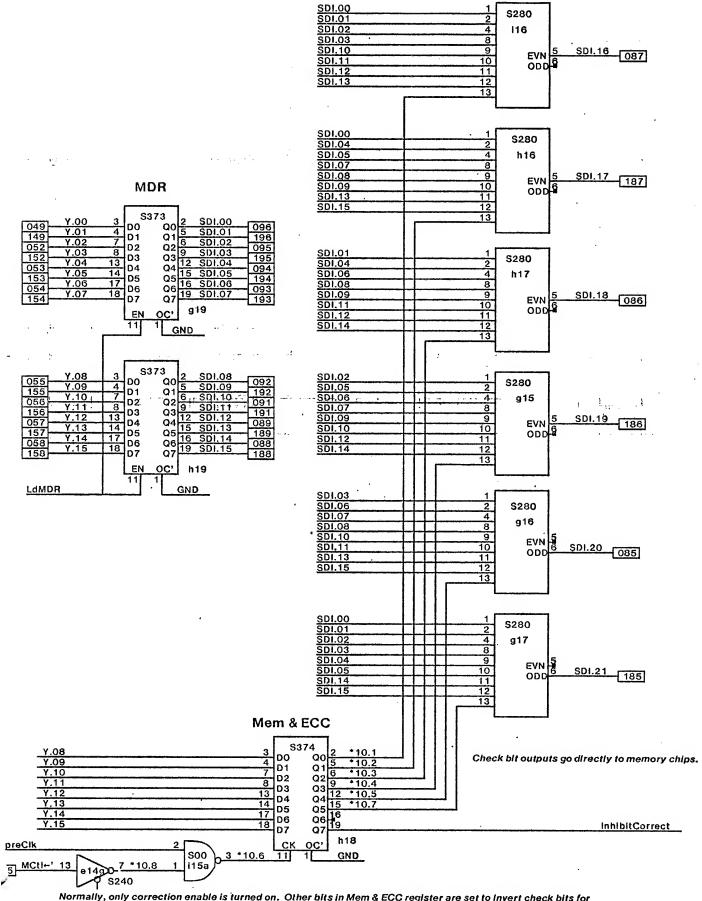
XEROX	Project		File	Designer	Rev	Date	Page
SDD	ws	Mem. Control/Low Bank B	EMCTL07.sil	Crane/Cucinitti	D	2/14/80	7
a galance state to the main	AND	and the second section of the property.		Spinger the great the second			Manageria By And Bridging



XEROX	Project		File	Designer	Rev	Date	Page
SDD	ws	Mem. Control/ Low Bank C	EMCTL08.sil	Crane/Cucinitti	D	2/14/80	8
Service Stand to be	AND THE REST OF	Children programme with the company	Service	MATERIAL CONTROLS CHARLES AND THE			



٠	XEROX	Project	_	File	Designer	Rev	Date	Page
	SDD	ws	Mem. Control/ Low Bank D	EMCTL09.sil	Crane/Cucinitti	D	2/14/80	9
-	Million of Contract of Springers of	AND THE STREET	The section of the Control of the	1.20	Contain in a pay in a man had		A fire the same	AND THE PERSON OF THE PERSON O

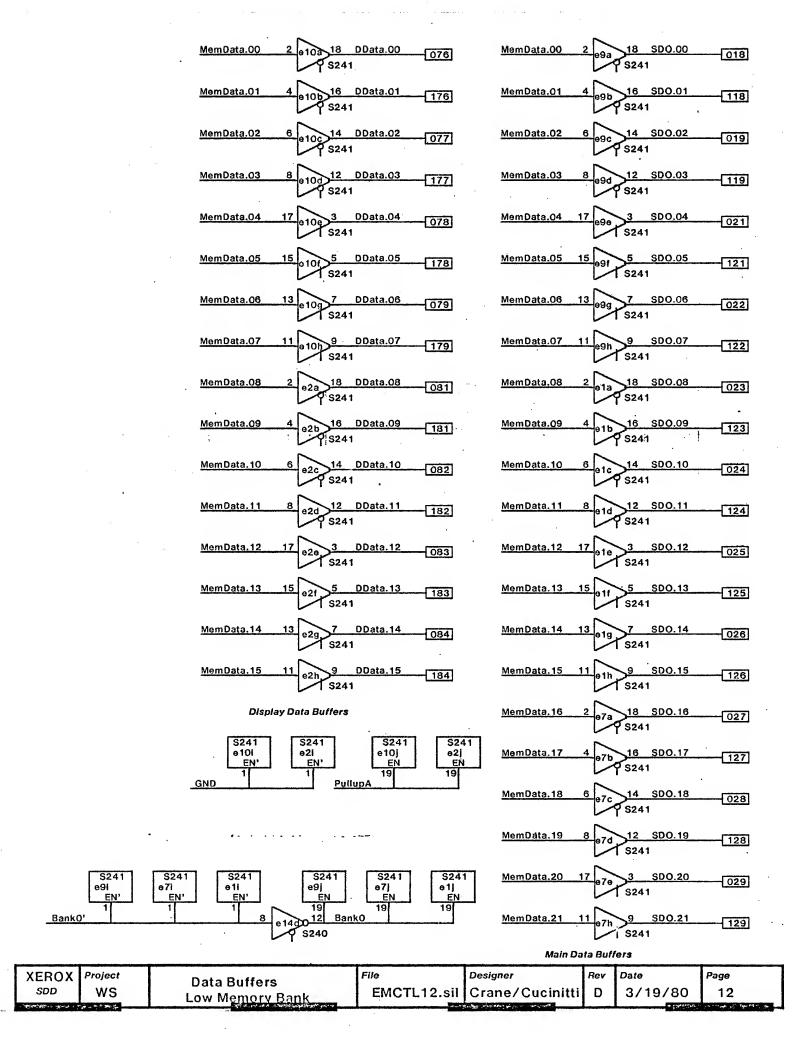


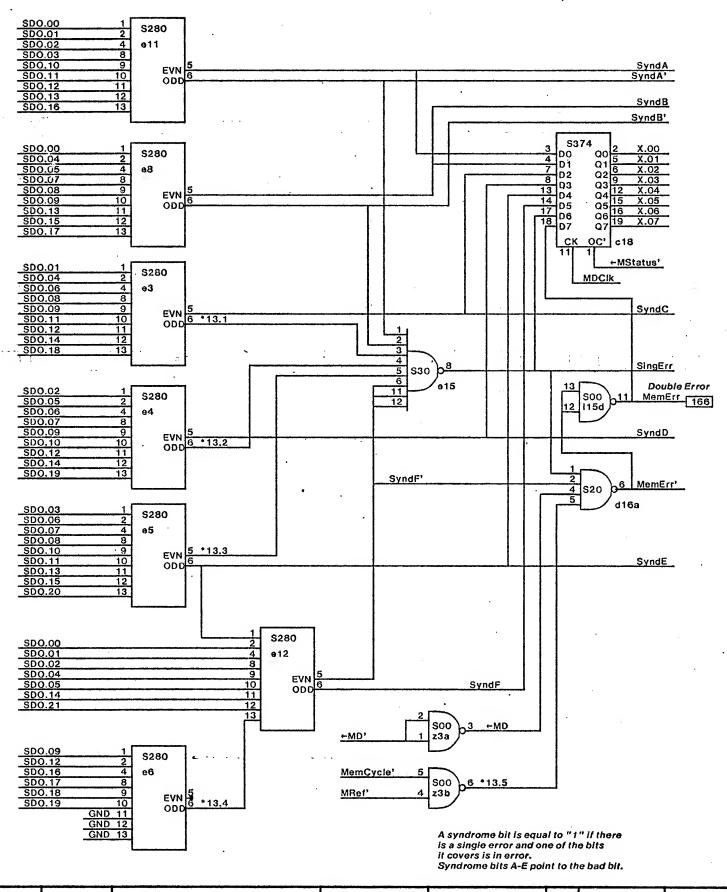
Normally, only correction enable is turned on. Other bits in Mem & ECC register are set to invert check bits for diagnostic purposes.

Data bits come from memory data register (MDR)

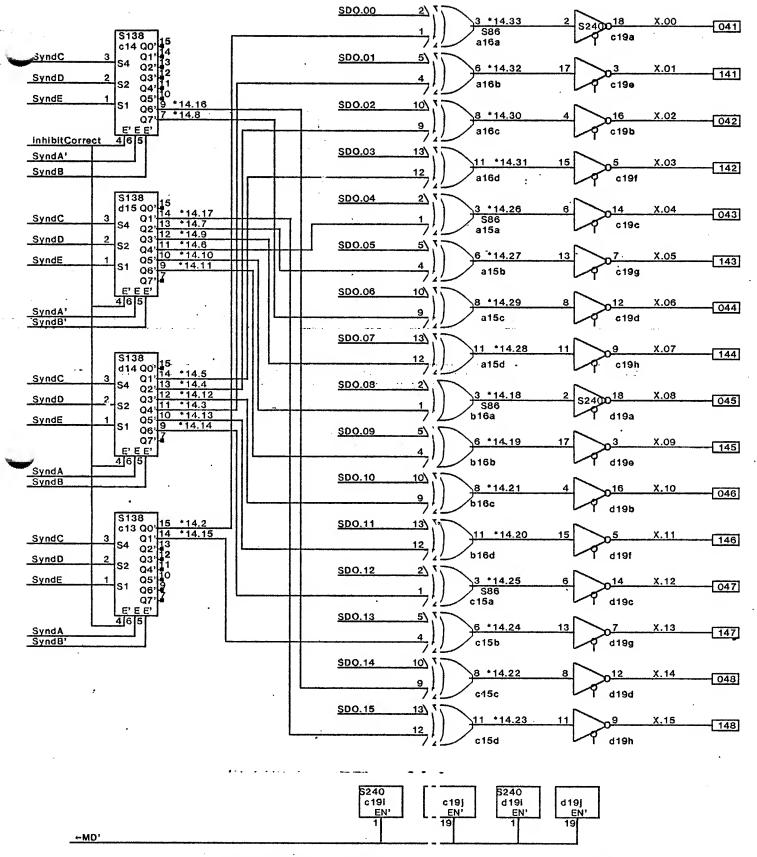
XEROX	Project	Mem. Data Reg., Mem. Ctl.	File	Designer	Rev	Date	Page
SDD	ws	Reg. & Check Bit Generator	EMCTL10.sil	Crane	D	2/14/80	10
A - MED OF WATER THE	Short die	and the same and the same and the same and		the state of the second		TV 80 843	agrangia del cer affici del kompaĝi

	SDI.00z 2	# %f12 114 MemData.00	2 # %I14	14 MemData.00	2 #%c1214	MemData.00	_2	#%b14 <mark>b4 M</mark> emi MK16-2	Data.00
	SDI.01z 2	# %f11 t/14 MemData.01 MK 16-2	J	14 MemData.01		MemData.01		# %b13 <u>b4 Meml</u> MK16-2	Data.01
	SDI.02z 2	# %110 114 MemData.02 MK 16-2	2 # %h12 MK16-2	14 MemData.02	2 # %d10d4 MK16-2	MemData.02		#%a12 <u>d4 Memi</u> MK16-2	Data.02
	SDI.03z 2	# %19 14 MemData.03 MK 16-2	2 # %i11 MK 16-2	14 MemData.03	2 # %d9b 14 MK 16-2	MemData,03	2	# %a11 d4 Memi	Data.03_
	SDI.04z 2	# %f8t <mark>14 MemData.04</mark> MK 16-2	2 # %19b MK 16-2	14 MemData.04	2 # %c8t14 MK16-2	MemData.04	2	# %a9b 14 Memi MK 16-2	Data.04_
	SDI.05z 2	# %171 <mark>14 MemData.05</mark> MK 16-2	2 # %h8t MK16-2	14 MemData.05	2 #%d7t14 MK16-2	MemData.05	2	# %a8b 14 Memi MK 16-2	Data.05_
	SDI.06z 2	# %16114 MemData.06 MK 16-2	2 # %17b MK 16-2	14 MemData.06	2 # %d6t14 MK 16-2	MemData.06	<u></u>	# %a7b 14 Mem! MK16-2	Data.06_
	SD1.07z 2	#%151 <mark>14 MemData.07</mark> MK 16-2	2 # %i6b MK 16-2	14 MemData.07	2 # %d5h14 MK16-2	MemData.07	2	# %a6t14 Memi MK 16-2	Data.07
	SD1.08z 2	# %14 b 14 MemData.08 MK 16-2	2 # %i4b MK 16-2	14 MemData.08	2 #%d4h14 MK16-2	MemData.08	2	# %a4b 14 Memi MK16-2	Data.08_
1.4	SDI.09z 2	# %13b 14 MemData.09 MK 16-2	2 # %i3b MK 16-2	14 MemData.09	2 #%d3l14 MK16-2	MemData.09	2	# %a3b <mark>14_Meml</mark> MK 16-2	Data.09
	SDI.10z 2	# %f2b14 MemData.10 MK16-2	2 # %i2b MK 16-2	14 MemData.10	2 #%d2t14 MK16-2	MemData.10	2 	# %a2b 14 Memi MK 16-2	Data.10
	SDI.11z 2	# %11b 14 MemData.11 MK 16-2	2 # %I1b MK 16-2	14 MemData.11	2 # %d1114 MK 16-2	MemData.11	2	# %a1b 14 Memi MK 16-2	Data.11_
	SDI.12z 2	# %g1t14 MemData.12 MK 16-2	2 # %h1i MK16-2	14 MemData.12	2 #%c1t14 MK16-2	MemData.12	2	#%b1b14 Memi MK16-2	Data.12
	SDI.13z 2	# %g2t14 MemData.13 MK16-2	2 # %h2b MK 16-2	14 MemData.13 "	2 #%c2t14 MK16-2	MemData,13	2	#%b2t14 Memi MK16-2	Data.13_
	SDI.14z 2	# %g3t <mark>14 MemData.14</mark> MK 16-2	2 # %h3b MK16-2	14 MemData.14	2 #%c3t14 MK16-2	MemData.14	2	# % b 3 b 1 4 Mem l MK 16-2	Data.14_
	SDI.15z 2	# %g4t 14 'MemData.15 MK 16-2	2 # %h4t MK 16-2	14 MemData.15	2 #%c4r14 MK16-2	MemData.15	2	# %b4b14 Mem MK16-2	Data. 15
	SDI.16z 2	# %g5t14 MemData.16 MK 16-2	2 # %h5t MK 16-2	14 MemData, 16	2 #%c5H14 MK16-2	MemData.16	2	#%b5h14 Meml MK 16-2	Data.16_
	SDI.17z 2	# %g6t <mark>14 MemData.17</mark> MK 16-2	2 # %h6t MK 16-2	14 MemData.17	2 # %c6t 14 MK 16-2	MemData.17	2	#%b6b14 Memi MK 16-2	Data. 17_
	SDI.18z 2	# %g7t14 MemData.18 MK 16-2	2 .# %h7b MK16-2	14 MemData,18	2 #%c7t14 MK16-2	MemData.18	2	#%b7b14 Memi	Data. 18_
	SDI.19z 2	# %g9t14 MemData.19 MK16-2	2 # %g8t MK 16-2	14 MemData. 19	2 #%b8b14 MK16-2	MemData.19		#%b9b14 Memi	Data.19_
	SD1.20z 2	# %g10154 MemData.20 MK16-2	2 # %h9h MK 16-2	14 MemData.20	2 # %c9t14 MK 16-2	MemData.20	2	# %b10 <u>84 Mem</u> MK16-2	Data.20
	SDI.21z 2	# %g1 1b4 MemData.21 MK 16-2	2 # %h10 MK 16-2	d 4 MemData.21	2 # %c1014 MK16-2	MemData.21	2	#%b11b4 Mem MK16-2	Data.21
XEROX	Project			File	Designer	Rev	Date	e Page	9
SDD	ws	Work Station Memory Bank()		EMCTL11.s		I			1
APATON ARE	or production and the	Menory Bank()	Marie and States		THE STREET			The State of the Control	and the same





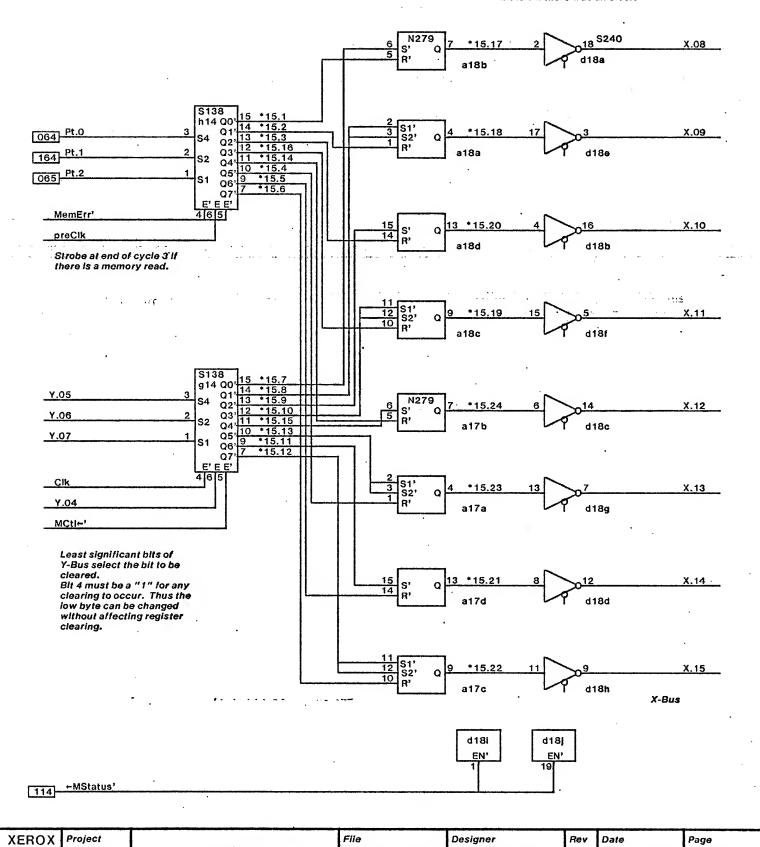
XEROX Project Designer Rev Date Page SDD **Syndrome Generator** WS EMCTL13.sil Crane D 2/14/80 13 व्यक्तिकार्याः स्टब्स The property and an interest are in-



Syndrome Bits point to the bad bit. SyndA is most significant bit & SyndE is LSB. Syndrome bit is a '1' if one of the bits it cove rs is in error.

	XEROX	Project		File	Designer	Rev	Date	Page
I	SDD	ws	Error Correction Data Paths	EMCTL1-41.sil	Crane	D	2/14/80	14
ı	المارية المهار المعالم المعالم المنطوات	A SECTION	the state of the state of the state of the state of		Section and section of the section of the			TOTAL AT TRANSPORTER STANDARDS TO

Errors Register
Bit is 1 if there was an error.



EMCTL15.sil

Crane

2/14/80

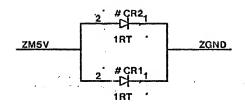
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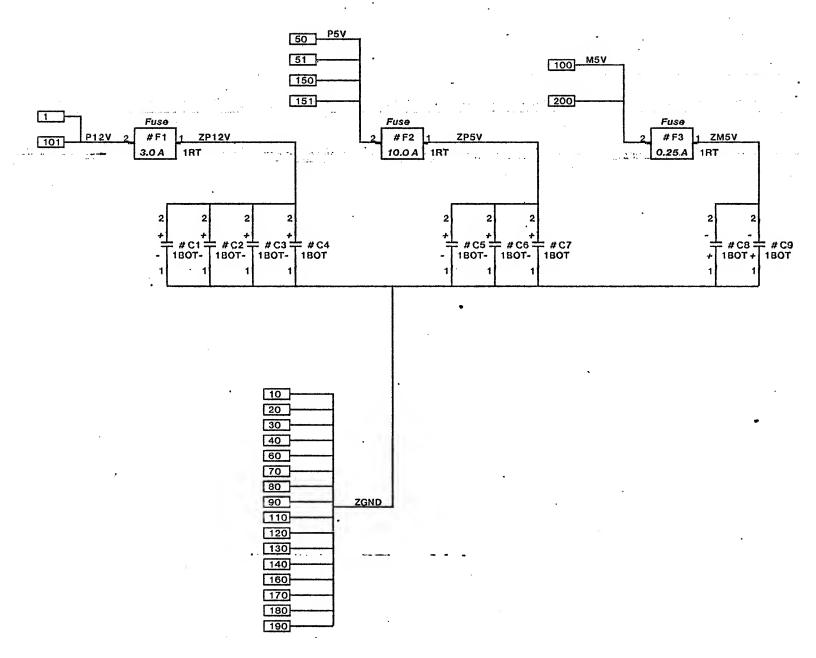
SDD

WS

Error Log Register

* SDI 00	2* #R1 1	SDI.00z	CASA'	2· #R24 ₁	CASAz'	CASC'	2* #R44 ₁	CASCz'
SDI.00	1RT .	501.002		1RT *			1RT #P45	
SDI.01	2· #R2 1	SDI.012	WriteA'	2. #R25 ₁	WriteAz'	WriteC'	2. #R45 ₁	WriteCz'
3	1RT *	0.	AAddr.00'	2. #R26 ₁	AAddr.00z'	CAddr.00'	2· #R46 ₁	ÇAddr.00z'
501.02	2· #R3 1	SDI.02z	AAGGIOO	1RT	AMOGINOUL	<u> </u>	1RT	<u> </u>
001.00	1RT 2 #R4 1	001.00-	RASA'	2. #R27 ₁	RASAz'	RASC'	2· #R47 ₁	RASCz'
SDI.03	1RT '	SDI.03z		1RT '	·		1RT *	
SDI.04	2* #R5 1	SDI.04z	<u>A Addr.03'</u>	2· #R28 ₁	AAddr.03z'	CAddr.03'	2· #R48 ₁	CAddr.03z'
	1RT		AAddr.06'	2. #R29	AAddr.06z'	CAddr.06'	2 #R49 ₁	CAddr.06z'
SDI.05	2· #R6 1	SD1.05z		1RT '			1RT ·	
SDI.06	2* #R7 1	SDI.06z	AAddr.02'	2. #R30 ₁	AAddr.02z'	CAddr.02'	2· #R50 ₁	CAddr.02z'
301.00	1RT	351.002		1RT			1RT *	
SDI.07	2· #R8 1	SDI.072	AAddr.04'	1RT	AAddr.04z'	CAddr.04'	1RT '	CAddr.04z'
	1RT *		AAddr.01'	2· #R32 ₁	AAddr.01z'	CAddr.01'	2. #R52 ₁	CAddr.01z'
SDI.08	2· #R9 1 1RT	SDI.08z		1RT			" · · · · 1RT '	
SDI.09	2*,#R10 ₁	\$D1.09z	AAddr.05'	2· #R33 ₁	AAddr.05z'	CAddr.05'	2· #R53 ₁	CAddr.05z'
•	1RT			1RT*			··-···· 1RT ·· '····	
SDI.10	2· #R11 ₁	SDI.10z	CASB'	2· #R34 ₁	CASBz'	CASD'	2 #R54 ₁	CASDz'
	1RT		W 44 - D1	2* #R35 ₁	•	W.O. B.	1RT 2* #R55 ₁	
SDI.11	2· #R12 ₁	SDI.11z	WriteB'	1RT '	WriteBz'	WriteD'	1RT .	WriteDz'
	1RT *		BAdd r.00'	2. #R36 ₁	BAddr.00z'	DAddr.00'	2* #R56 ₁	DAddr.00z'
CO1. <u>12</u>	2· #R13 ₁	SDI.12z		1RT *		•	1RT '	
SDI.13	2· #R14 ₁	SDI.13z	RASB'	2* #R37 ₁	RASBz'	RASD'	2· #R57 ₁	RASDz'
	1RT		BAddr.03	2· #R38 ₁	BAddr.03z'	DAddr.03'	2* #R58 ₁	DAddr.03z'
SDI.14	2· #R15 ₁	SDI.14z	3,000,00	1RT '		311331133	1RT '	
SDI.15	2* #R16 ₁	SDI.15z	BAddr.06'	2· #R39 ₁	BAddr.06z'	DAddr.06'	2· #R59 ₁	DAddr.06z'
301.10	1RT	351.132		1RT '			1RT # 860.	
SDI.16	2· #R17 ₁	SDI.16z	BAddr.02'	2· #R40 ₁	BAddr,02z'	DAddr.02'	2· #R60 ₁	DAddr.02z'
40	1RT ************************************		BAddr.04'	2· #R41 ₁	BAddr.04z'	DAddr.04'	2. #R61 ₁	DAddr.04z'
SDI.17	1RT .	SDI.17z		1R T			1RT '	
SDI.18	2· #R19 ₁	SDI.18z	BAddr.01'	2· #R42 ₁	BAddr.01z'	DAddr.01'	2: #R62 ₁	DAddr.01z'
	1RT		BAddr.05'	2 #R43	BAddr.05z'	DAddr.05'	2. #R63 ₁	DAddr.05z'
SDI.19	2· #R20 ₁	SDI.19z		1RT			1RT	
SDI.20	2· #R21 ₁	SDI.20z			•	-		
<u> </u>	1RT	V211204			MemData, 1	<u> </u>	ULL16 = VCC	Mana Data de
SDI.21	2· #R22 ₁	SDI.21z		• •	MemData.1 MemData.2	$\frac{8}{0}$ RP2	RP15 14 13	MemData.15 MemData.17 MemData.19
_	1RT *		MemData.00 1	RPULL16		5- RP4 RP5	RP13 13	MemData.19
<u>PullupA</u>	2· #R23 ₁	ZP5V	MemData.02 2 MemData.04 3	RP1 = VCC RP2 RP15	15 MemData. 14 MemData.	일 7 RP7	RP12 RP11 10 RP10 9 RP9	
PullupB	2· #R64 ₁	ZP5V	MemData.06 4 MemData.08 5	RP4 RP13	13 MemData. 12 MemData.	05 07	-2	D 16
	1RT ·	• • • • • • • • • • • • • • • • • • • •	MemData.10 6 MemData.12 7	RP6 RP11	l 1 MemData. 10 MemData.	<u>11</u>	*	D 16 z1x
RFCL	2· #R65 ₁	ZP5V	MemData.14 8	RP8 RP9	9 MemData.	<u>13</u>	GN	D 16 z2x
VEDO	1RT '			File	Daci	In.	Insta	I Page
XEROX SDD	Project WS	RESISTORS	AND R - DIPS		Designer sil Crane/C	Rev Cucinitti D	Date 2/14/80	Page 16
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1	VEDOV	Project		File	Daniman	Rev	Date	Cara
	XEROX SDD	WS	CAPS, DIODES and FUSES		Designer Crane/Cucinitti			Page 17
				2	Grano, Gadinieti		27	

```
CASA'
                                              SDI.00z
           <u>1</u>-⊚ tI #TP001
                                                           <u>1</u> ⊚ ti #TP041
                                                                                          MemData.00
                                                                                                      <u>-1</u>-⊚ tI #TP063
WriteA'
           SD1.012
                                                           <u>1</u> ⊚ tI #TP042
                                                                                          Mem Data.01
                                                                                                      MemData.02 1 () tl #TP065
AAddr.00'
                                              SDI.02z
           <u>1</u>-⊚ ti #TP043
                                                                                          MemData.03 1 () tl #TP068
RASA'
                                              SDI.03z
           <u>1</u>-⊚ tI #TP044
AAddr.03'
                                               SDI.04z
                                                                                          MemData.04
           <u>1</u>_@ tl=#TP005
                                                           <u>1</u> ⊚ ti #TP045
                                                                                                      MemData.05 1 () ti #TP068
AAddr.06'
                                              SDI.05z
           MemData.06 1 © tl #TP069
AAddr.02'
           SDI.06z
                                                           <u>1</u>-⊚ tI #ŢP047
                                                                                          MemData.07 1 (1) tl #TP070
AAddr.04'
           <u>1</u>-⊚ tl #TP008
                                              SDI.07z
                                                           1_© ti #TP048
                                                                                          MemData.08 1 ( tl #TP071
AAddr.01'
                                              SDI.08z
           <u>1</u>-⊚ tI #TP009
                                                           MemData.09 1 © tl #TP072
                                              SDI.09z
AAddr.05'
           <u>-1</u>-⊚ tI #TP010
                                                           MemData.10 1 (1) #TP073
                                               SDI.10z
                                                           <u>-1</u>-⊚ ti #TP051
                                                                                          MemData.11 1 0 tl #TP074
CASB'
                                              SDI.11z
           <del>1</del>_⊚ tI #TP011
                                                           WriteB'
                                              SDI.12z
           <u>1</u>-⊚ tI #TP012
                                                           BAddr.00'
                                              SDI.132
           <u>-1</u>-⊚ tI #TP013
                                                           <u>1</u> ⊚ tI #TP054
                                                                                          MemData.14 1 (1) tl #TP077
RASB'
                                              SDI.14z
           <u>1</u>_⊚ tI #TP014
                                                           BAddr.03'
           SDI.152
                                                           MemData.16 1 0 tl #TP079
BAddr.06'
           SDI.162
                                                           1 (0 ti #TP057
                                                                                          MemData.17 1 0 tl #TP080
BAddr.02'
                                              SDI.17z
           <u>1</u> ⊚ ti #TP058
                                                                                         BAddr.04'
                                              -SDI.18z
                                                          <u>1</u> ⊚ ti #TP059.
           MemData.19 1 (1) tl #TP082
BAddr.01'
                                              SDI.19z
                                                           1_@ tl #TP060
           <del>1</del>_⊚ tI #TP019
                                                                                         MemData.20 1 © tl #TP083
BAddr.05'
                                              SDI.20z
           SD1.21z
                                                           <u>-1</u>-⊚ tI #TP062
CASC'
           <del>1_</del>@ tI #TP021
WriteC'
           CAddr.00'
           <u>1</u>-⊚ tI #TP023
RASC'
                                               MCycle
           <del>1</del>_⊚ tI #TP024
                                                           <del>1</del>_⊚ tI #TP085
CAddr.03'
           <u>1</u>-⊚ tI #TP025
CAddr.06'
                                              LatchY.02
           <u>1</u>-⊚ tI #TP026
                                                           1 (O) tI # TP086
CAddr.02'
                                              LatchY.03
           RFCL
CAddr.04'
                                                                                                         - ○ tl #TP098
                                              LatchY.05
           <u>-1</u>-⊚ tI #TP028
                                                           <u>1</u>-⊚ ti #TP088
CAddr.01'
                                              LatchY.06
           <del>1</del>_⊚ tI #TP029
                                                           1 (O) ti #TP089
                                                                                          PullupB
                                                                                                       <del>1</del>-⊚ tI #TP099
CAddr.05'
           LatchY.07
                                                           <u>1</u> ⊚ tI #TP090
                                              LatchY.08
                                                           <u>-1</u>-⊚ tI #TP091
CASD'
           <u>-1</u>-⊚ tI #TP031
                                              LatchY.09
                                                           <del>_1_</del>⊚ tI #TP092
WriteD'
           LatchY.10
                                                           <u>-1</u>-⊚ tI #TP093
DAddr.00'
           <u>-1</u>-⊚ tI #TP033
                                              LatchY.11
                                                           <u>-1</u>-⊚ tI #TP094
RASD'
           <del>1</del>-⊚ tI #TP034
                                              LatchY.13
                                                           <u>1</u>-⊚ tI #TP095
DAddr.03'
           <u>1</u>-⊚ tI #TP035
                                              LatchY.14
                                                           <del>1</del>-⊚ tI #TP096
DAddr.06'
           <u>1</u> ⊚ ti #†P036
                                              LatchY,15
                                                           <del>1</del>_⊚ tI #TP097
DAddr.02'
           <u>-1</u>-⊚ tI #TP037
DAddr.04'
           <del>1</del>_@ tI #TP038
DAddr.01'
           <u>1</u> ⊚ ti #TP039
DAddr.05'
           <del>_1</del>_⊚ tI #TP040
```

XEROX	Project	TEST	POINTS	File	Designer	Rev	Date Page		
SDD	ws			EMCTL18.sil	Crane/Cucinitti	D	3/19/80	18	
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1 2 3 4 5 6 7 2 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	INTEGRATED CIRCUIT SN74S00 INTEGRATED CIRCUIT SN74S02 INTEGRATED CIRCUIT SN74S04 INTEGRATED CIRCUIT SN74S10 INTEGRATED CIRCUIT SN74S20 INTEGRATED CIRCUIT SN74S30 INTEGRATED CIRCUIT SN74S37	733w00318 733w01643 733w00319 733w01606 733w01619 733w01645	3 3 1 3	·
3 4 5 6 7	INTEGRATED CIRCUIT SN74\$04 INTEGRATED CIRCUIT SN74\$10 INTEGRATED CIRCUIT SN74\$20 INTEGRATED CIRCUIT SN74\$30	733w00319 733w01606 733w01619	. 1	·
4 5 6 7	INTEGRATED CIRCUIT SN74S10 INTEGRATED CIRCUIT SN74S20 INTEGRATED CIRCUIT SN74S30	733w01606 733w01619	<u> </u>	
5 6 7	INTEGRATED CIRCUIT SN74S20 INTEGRATED CIRCUIT SN74S30	733w01619	3	
6 7	INTEGRATED CIRCUIT SN74\$30			
7		733w01645	1	
	INTEGRATED CIRCUIT SN74S37	, , , , , , , , , , , , , , , , , , , ,	1	
		733w02136	1	
8 .	INTEGRATED CIRCUIT SN74S74 .	733w01771	2 .	
9	INTEGRATED CIRCUIT SN74S86	733w01648	4	
10	INTEGRATED CIRCUIT SN74S138	733w01616	6	
11	INTEGRATED CIRCUIT SN74S139	733w01669	1	
12	INTEGRATED CIRCUIT SN74S240	733w01633	9	
13	INTEGRATED CIRCUIT SN74S241	733w01634	5	
14	INTEGRATED CIRCUIT SN74S253	733w01636	8	
15	INTEGRATED CIRCUIT SN74279	733w00341	2	
. 16	INTEGRATED CIRCUIT	733w01638	-13-	
17	INTEGRATED CIRCUIT . SN74S373	733w01699	4	·
18	INTEGRATED CIRCUIT \$N74S374	733w01640	2	
19	INTEGRATED CIRCUIT SN74LS393	733w01663	1	
20	MEMORY CHIP 16K MK4116-2	.733w01512	88	
21	CAPACITOR 0.1uf 50v	102P20600	115	
22	CAPACITOR 20uf 15v	702W07301	5	C5>C9 (alt. 25uf 12v 702W05601)
23	CAPACITOR 10uf 25v	702W08901	4	C1> C4
24	DELAY LINE 25 ns Eng Components Co.	744W00001	2	X1 + X2 TTLDM025
25	DIODE 1N5820	107P10105	2	CR1 + CR2
26	FUSE 0.25 A	708W 10302	1	F3 .
27	FUSE 3.0 A	708W11002	1	F1
26	FUSE 10.0 A	708W11402	1	F2
29	R-DIP 1.0 k ohm	703W13291	2	Z1 + Z2
30	RESISTOR 18 ohm 1/4 watt 5 %	703W28088	12	R24,R25,R27,R34,R35,R37,R44,R45, R47,R54,R55 + R57
31	RESISTOR 20 ohm 1/4 watt 5%	703W28188	28	R26,R28> R33,R36,R38> R43, R46,R48> R53,R56,R58> R63
32	RESISTOR 27 ohm 1/4 watt 5 %	703W28488	22	R1> R22
33	RESISTOR 1.0 k ohm 1/4 watt 5%	703W32288	3	R23,R64 + R65
34	PWB	140P11229	1	
35	BOARD EXTRACTOR	003P80513	2	
36	STIFFENER (front)	596P54167	1	
37	STIFFENER (back)	030P83244	1	
38	RIVETS	320W 13201	7	

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Error Correction Logic

Code Table

The codes have been optimized for use with 9 input parity chips (\$280). Each row represents the inputs to a single chip. 8 inputs are used when writing and 9 are used when reading.

(Check bit F is parity over entire word. X's are omitted from the group of bits whose overall parity remains fixed.)

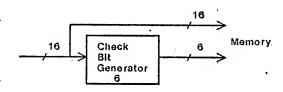
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	а	b	С	d	ө	f
a	x	x	x	×							×	x	×	x			×					
b	x				×	×		×	х	х				x		х		×				
c		x			x		×		×	×		х	x		х				x		П	
đ			х			×	x	х		х	х		x		х					×		
θ				х			x	x	×		x	х		х		х					×	
f	×	×	x	х	x	x									х	х						×
											•											
							Data	Bits	1									Che	ck Bi	ts		

Parity over all 22 bits

Writing

Check bits written into memory are parity calculated over the data bits in the corresponding row.

Check bits a-d are odd parity and bits e-f are even parity. Bit f is really parity over the whole word, but the number of bits directly used to generate bit F is only 8 since the other data bits are cancelled out by other check bits.



Parity checker chips Delay = 1.15 (21) = 24 n\$

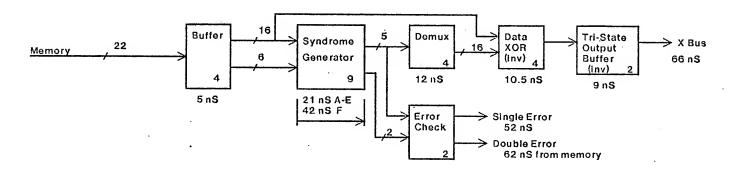
Reading

All bits from rows A-E are used for the corresponding syndrome bit.

(Stored parity: A-D = odd, E,F = even)

Check Bits

All 22 bits of the stored memory word are included in generation of syndrome bit F.



Numbers inside boxes are the number of chips used for the function.

Numbers below boxes are maximum delays from TI TTL Data book. 15% is added below to allow for board propagation time

Total Delay for Data = 1.15(57.5) = 66 nSor 61 nS without buffer

	Error Check Possibilities										
Sync	rome	Meaning									
OR A•F	Synd F										
0 0 1 1	0 1 0 1	No error or >2 errors Not Possible Dbi error detected Single error corrected									

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Map References

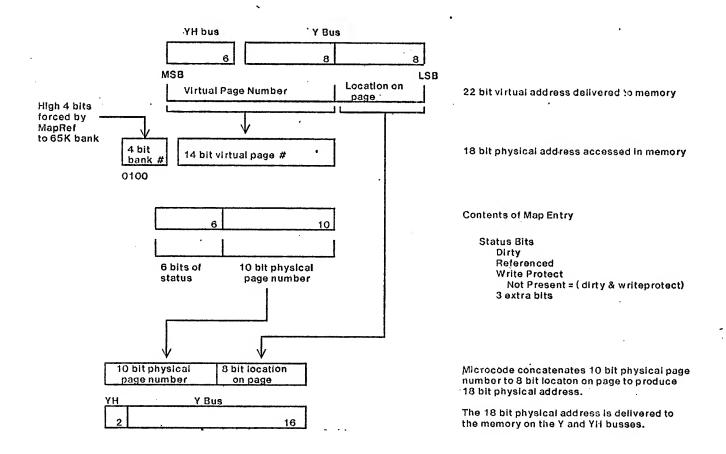
The memory system supports a 22 bit virtual address space divided into pages of 256 words each. Thus, 14 bits specify the page number and 8 bits specify the location within the page.

The physical memory system will support up to 256K of real memory, i.e. an 18 bit address space. Thus there is a 10 bit physical page number and 8 bits as above for specifying the location within the page.

Since the virtual space is larger than the physical space, a mapping is performed between the 14 bit virtual page number and the 10 bit physical page number. The 14 bit virtual page number is used to access one of 16K locations which comprise the map in main memory. The accessed memory location (map entry) contains the 10 bit physical page number and status bits for the page (write protect, referenced, dirty).

Map References to the memory system are done by specifying MapRef in the microcode and sending the 22 bit virtual memory address to the memory via the Y (16 bits) and YH (6 bits) busses.

This causes an access into the map, a 16K word segment of main memory located between 65K and 80K. Specifying MapRef forces access to the 65K-80K bank while the high 14 bits of the 22 bit virtual address are used to access a word within that 16K bank.



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